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**JK Lakshmipat University**

[**Computer**](https://canvas.instructure.com/courses/8496533) **Organization and Architecture**

**CLASS ASSIGNMENT**

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**Section – B**

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**Submitted To – Dr. Pranab Roy Sir**

**Question 1**

**An instruction format has the following structure:**

**Instruction Number: Opcode destination reg, source reg-1, source reg-2**

**Consider the following sequence of instructions to be executed in a pipelined processor:**

**I1: DIV R3, R1, R2**

**I2: SUB R5, R3, R4**

**I3: ADD R3, R5, R6**

**I4: MUL R7, R3, R8**

**Which of the following statements is/are TRUE? (explain with valid reasons)**

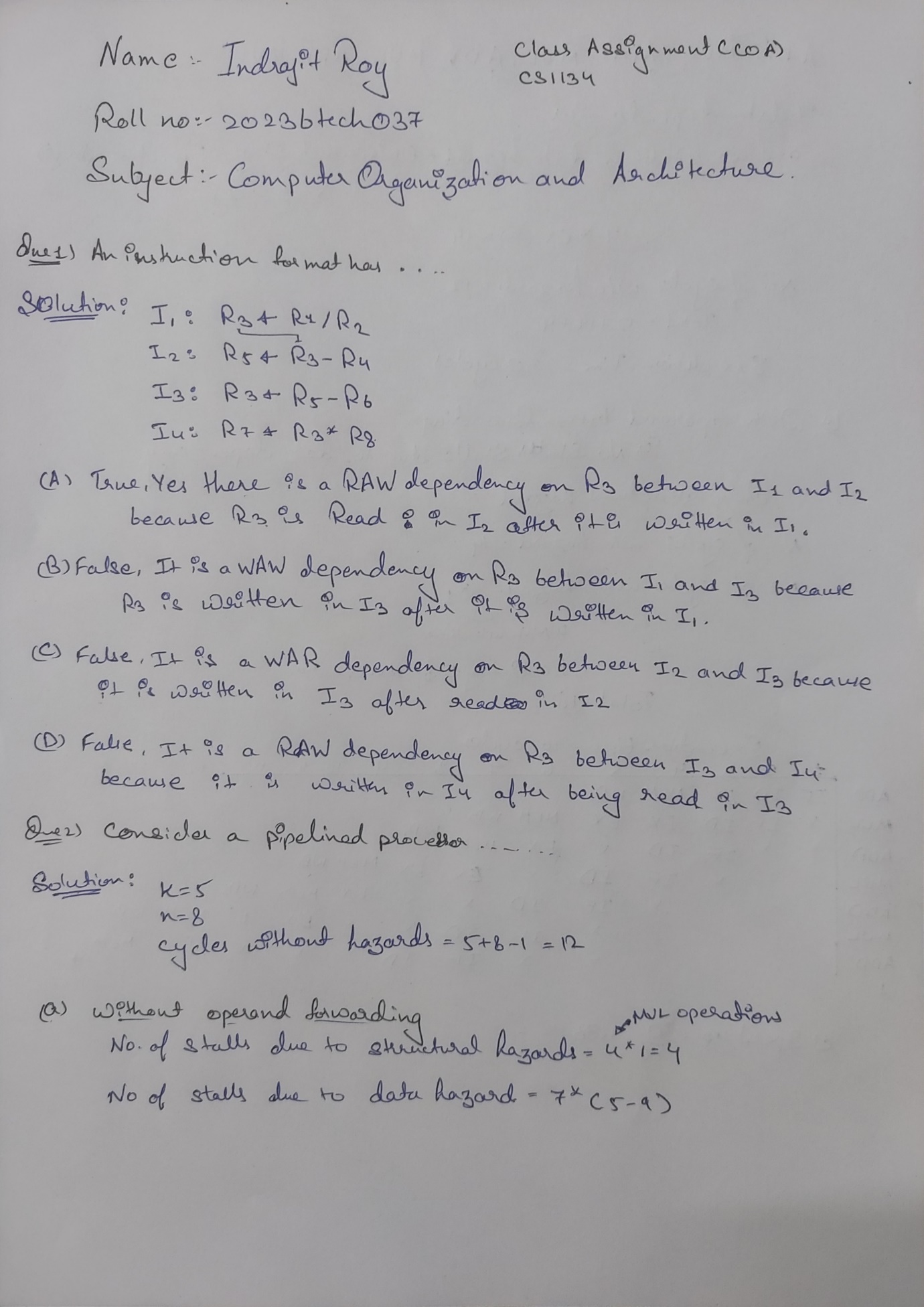
**A. There is a RAW dependency on R3 between I1 and I2**

**B. There is a WAR dependency on R3 between I1 and I3**

**C. There is a RAW dependency on R3 between I2 and I3**

**D. There is a WAW dependency on R3 between I3 and I4**

**Solution :**



**Question 2**

**Consider a pipelined processor with 5 stages, Instruction Fetch (IF), Instruction**

**Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Each stage of**

**the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely**

**decodes the instruction and the register read is performed in the EX stage. The EX stage**

**takes one cycle for ADD instruction and two cycles for MUL instruction. Ignore pipeline**

**register latencies.**

**Consider the following sequence of 8 instructions:**

**ADD, MUL, ADD, MUL, ADD, MUL, ADD, MUL**

**Assume that every MUL instruction is data-dependent on the ADD instruction just**

**before it and every ADD instruction (except the first ADD) is data-dependent on the**

**MUL instruction just before it. The speedup is defined as follows:**

**Speedup=**

**Execution time without operand forwarding /Execution time with operand forwarding**

**Find the**

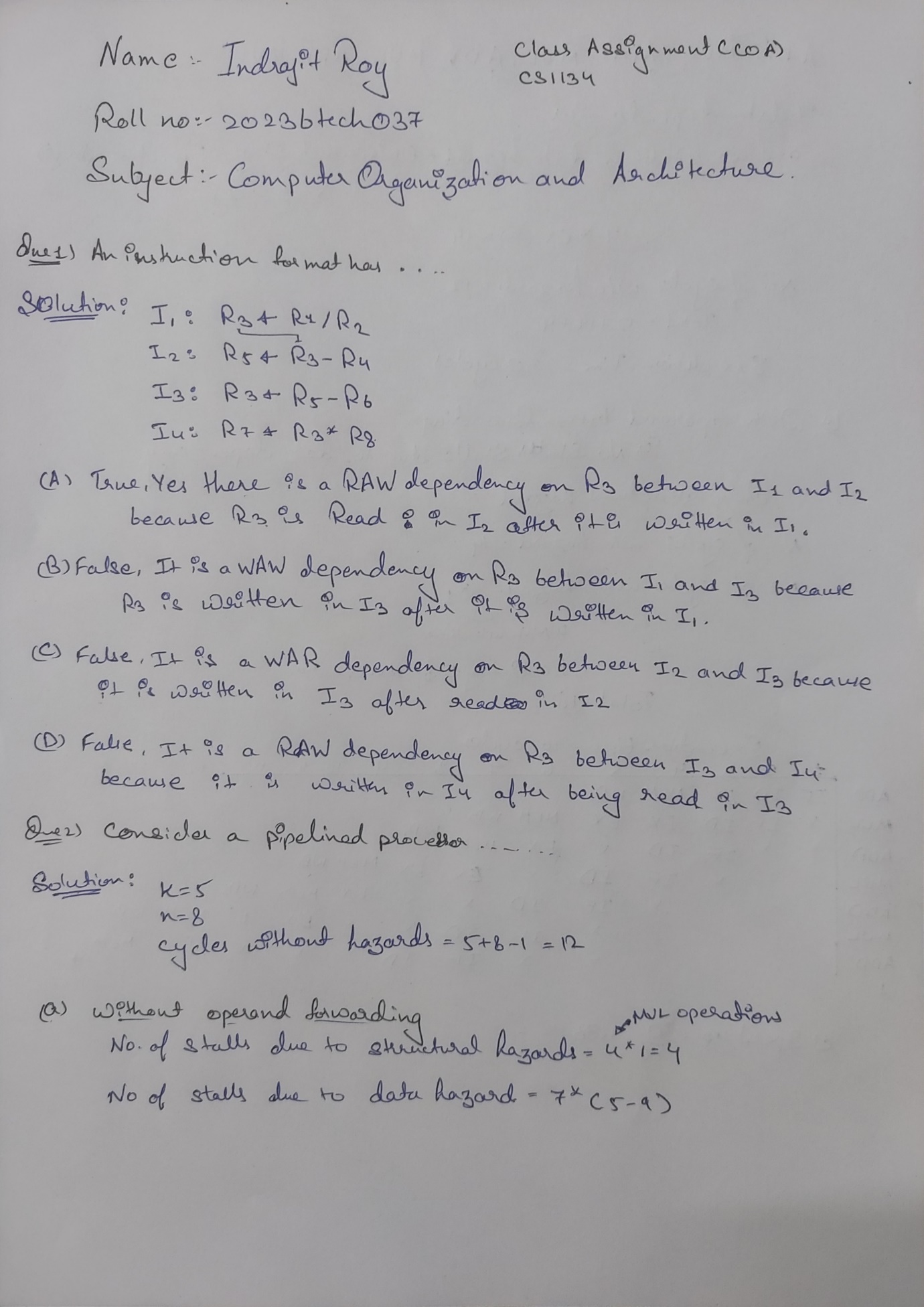
**a. Execution time without operand forwarding**

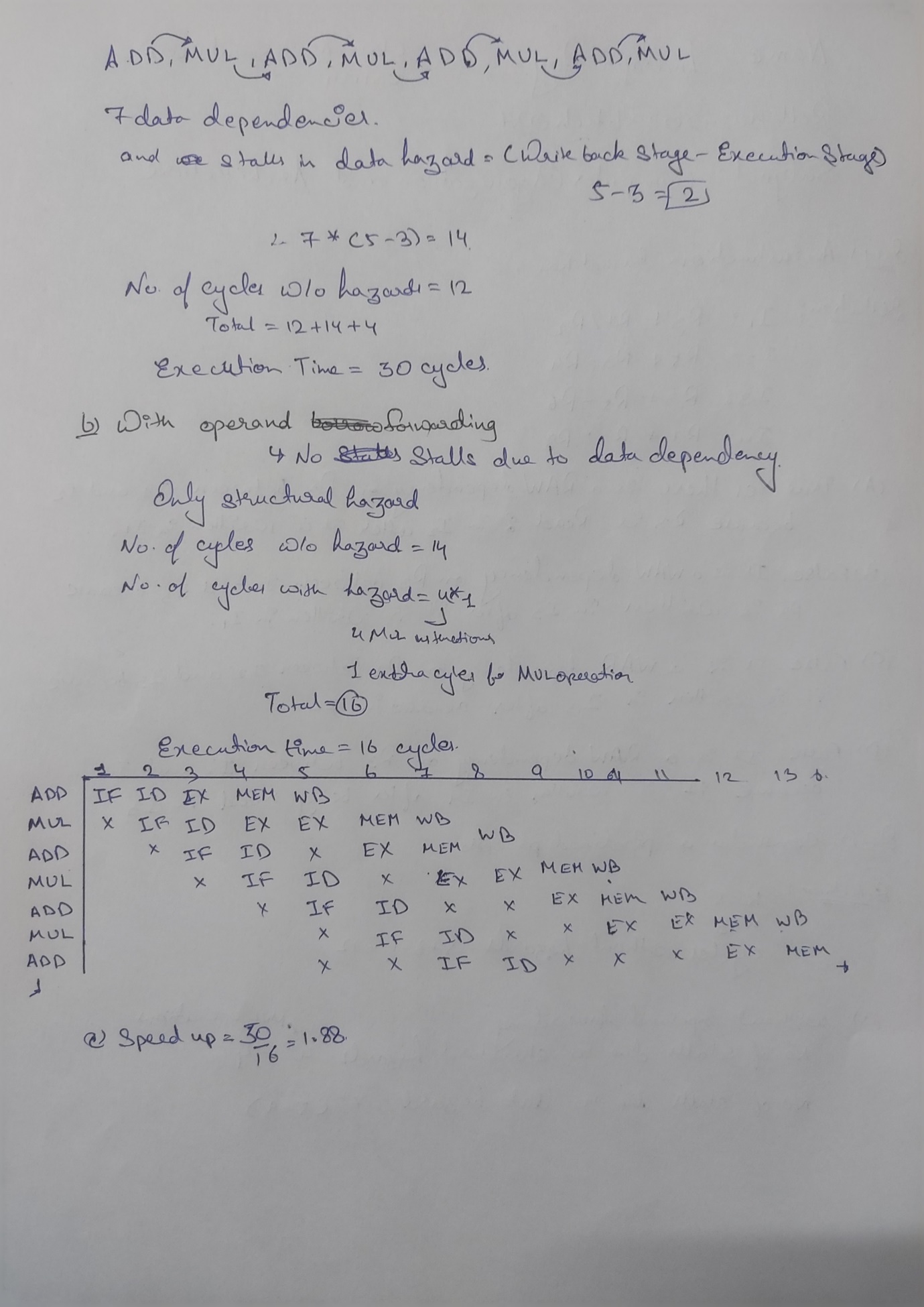
**b. Execution time with operand forwarding**

**c. The Speedup achieved in executing the given instruction sequence on the**

**pipelined processor (rounded to 2 decimal places).**

**Solution :**





**Question 3**

**Consider a direct mapped cache with 8 cache blocks (0-7). If the memory block**

**requests are in the order-**

**3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24**

**Which of the following memory blocks will not be in the cache at the end of the**

**sequence?**

**1.3**

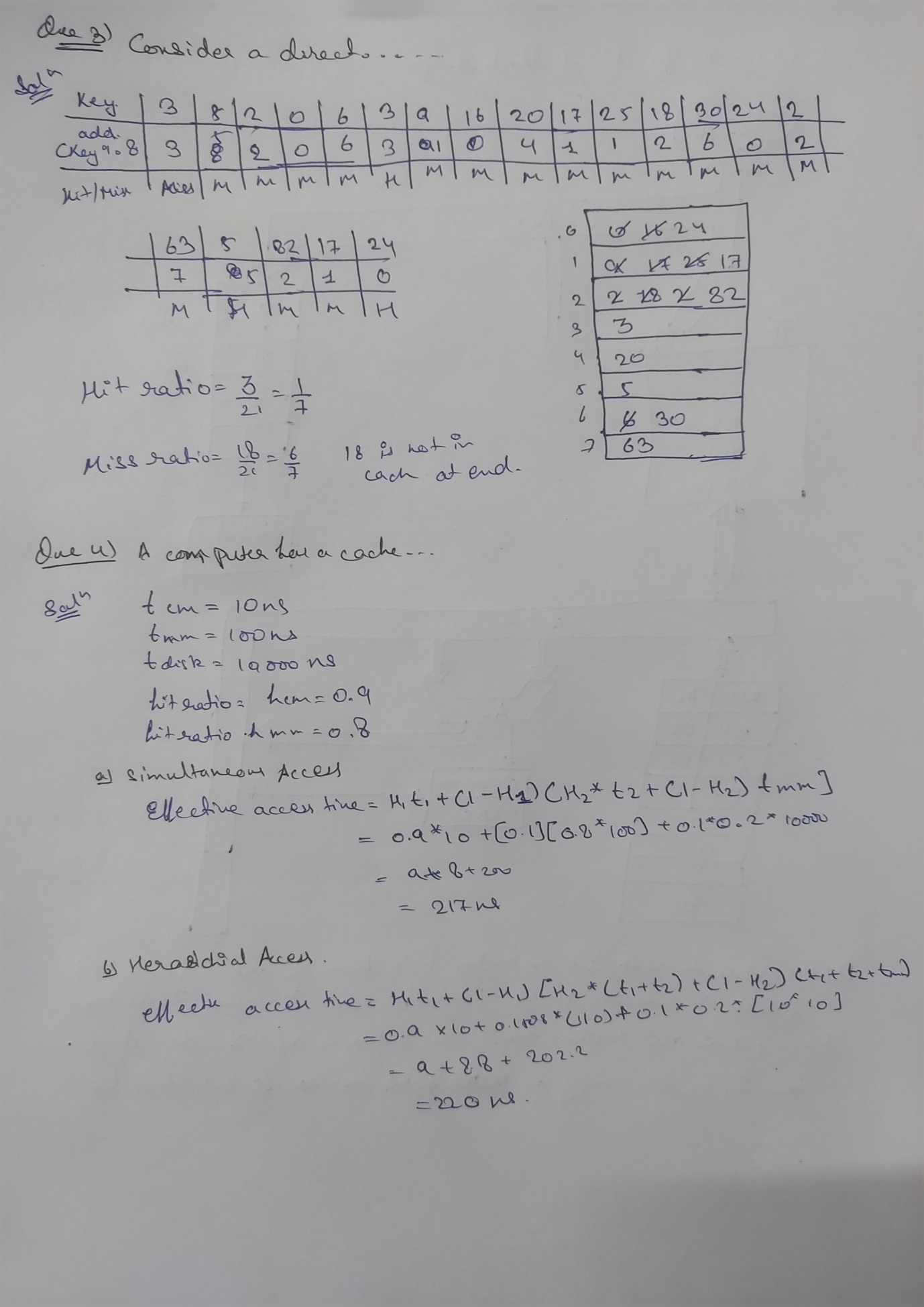
**2.18**

**3.20**

**4.30**

**Also, calculate the hit ratio and miss ratio.**

**Solution :**



**Question 4**

**A computer has a cache, main memory and a disk used for virtual memory. An access**

**to the cache takes 10 ns. An access to main memory takes 100 ns. An access to the disk**

**takes 10,000 ns. Suppose the cache hit ratio is 0.9 and the main memory hit ratio is 0.8.**

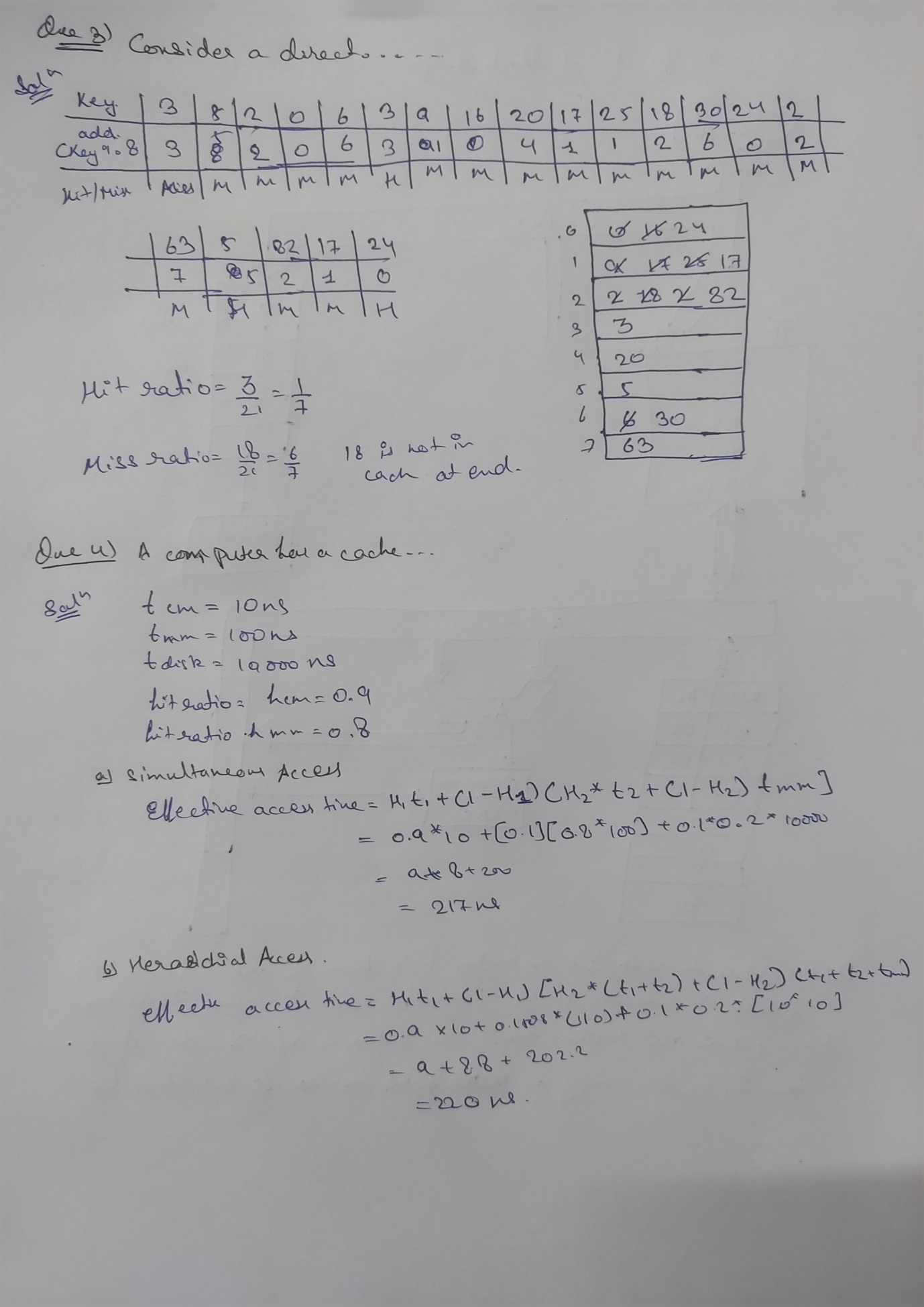
**The effective access time required to access a referenced word on the system is \_\_\_\_\_\_\_**

**when-**

**a. Simultaneous access memory organization is used.**

**b. Hierarchical access memory organization is used.**

**Solution :**



**Question 5**

**Draw the functional block diagram of 8086 microprocessor and describe instruction**

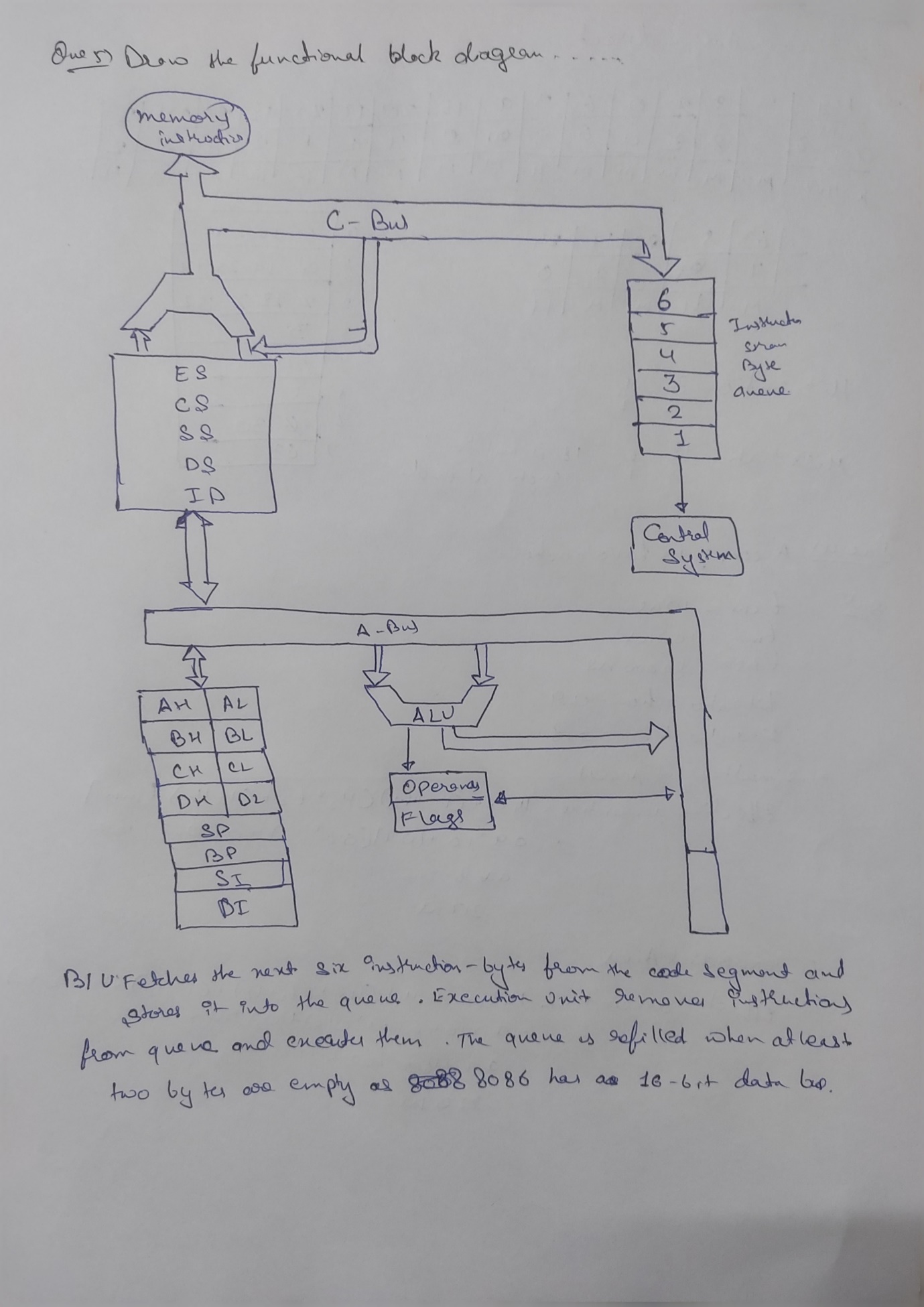
**queue in detail.**

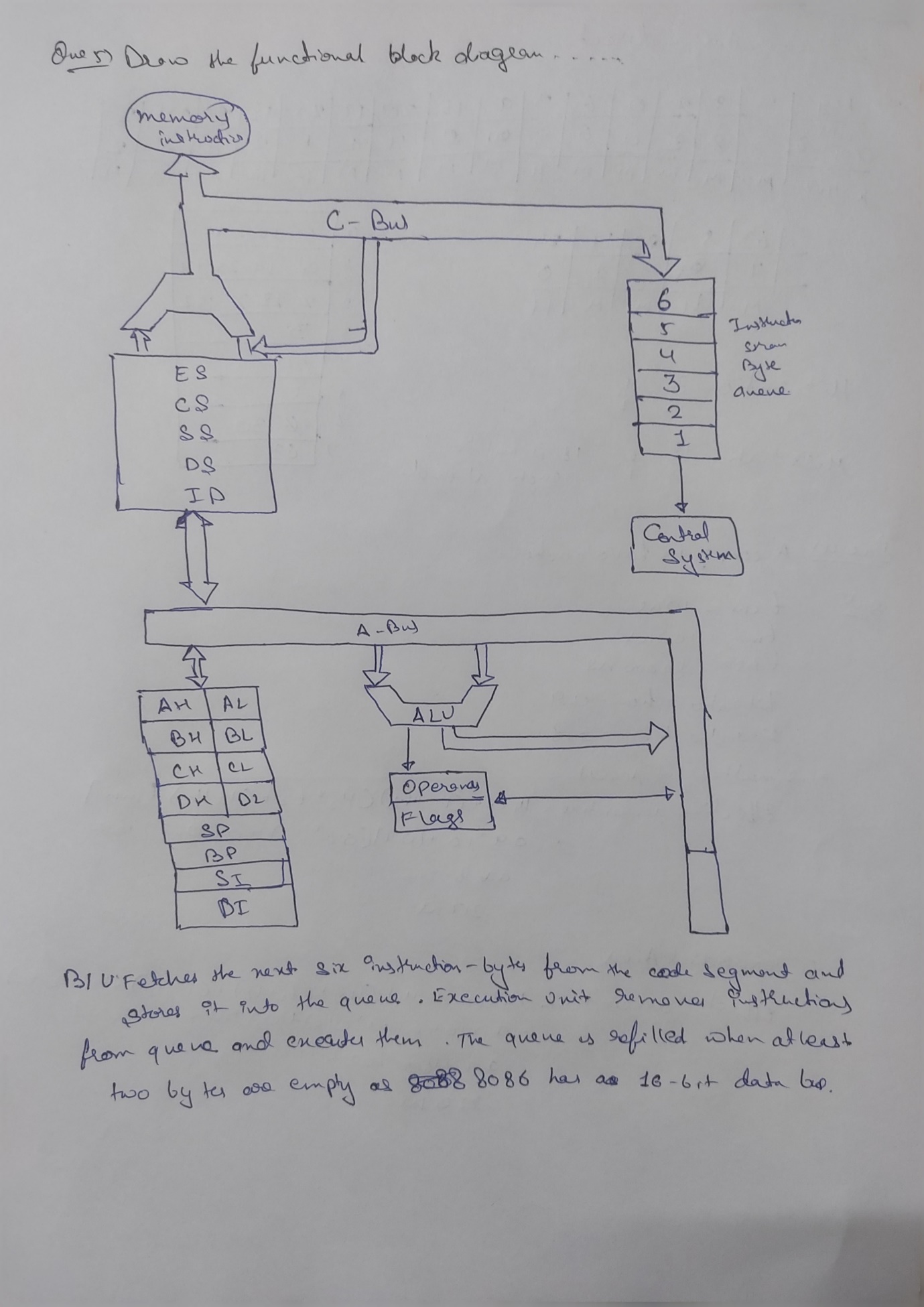
**Explain the concept of pipelining in 8086 microprocessors with diagram.**

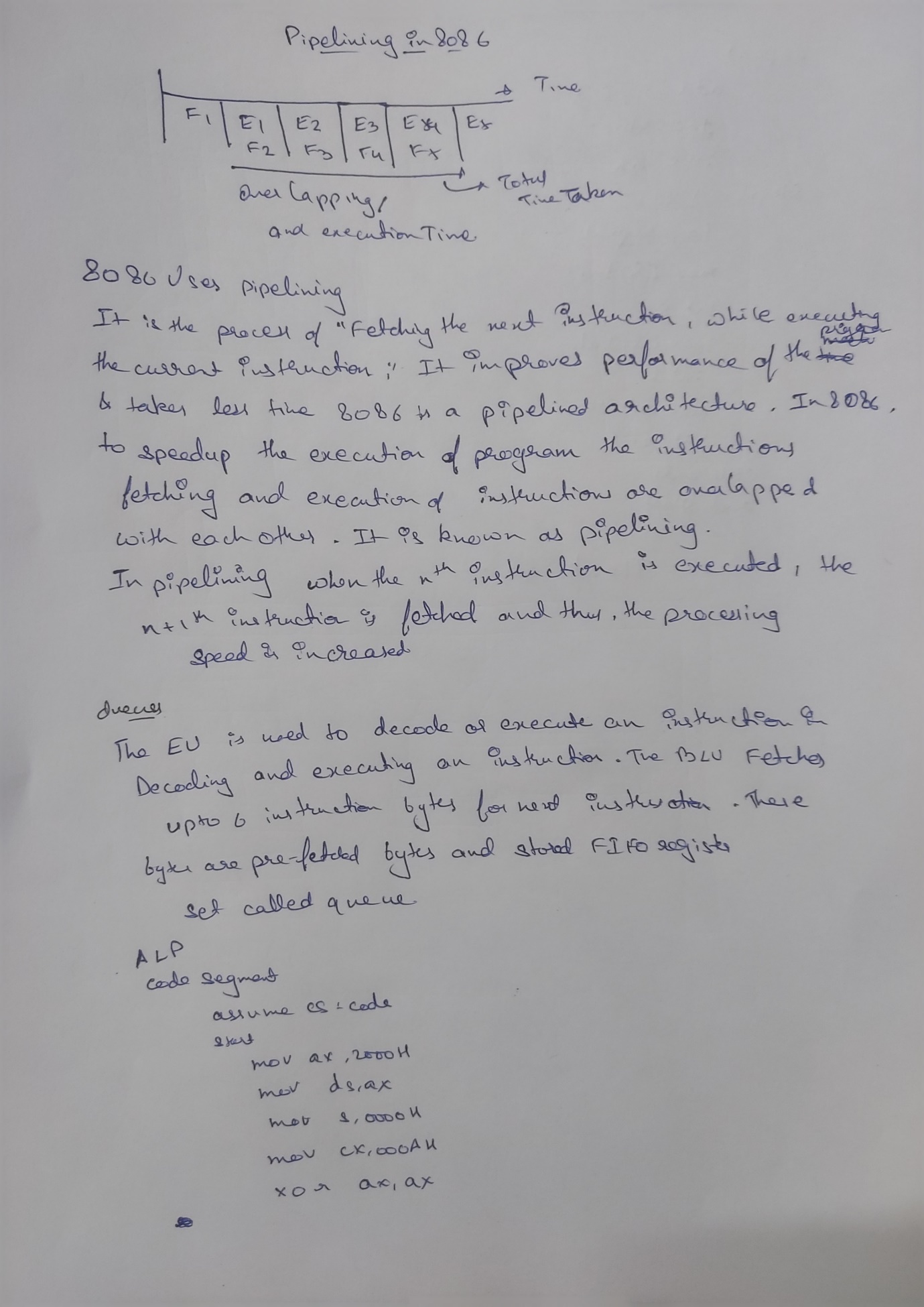
**Write an ALP to add a series of 10 bytes stored in the memory from locations 20,000H**

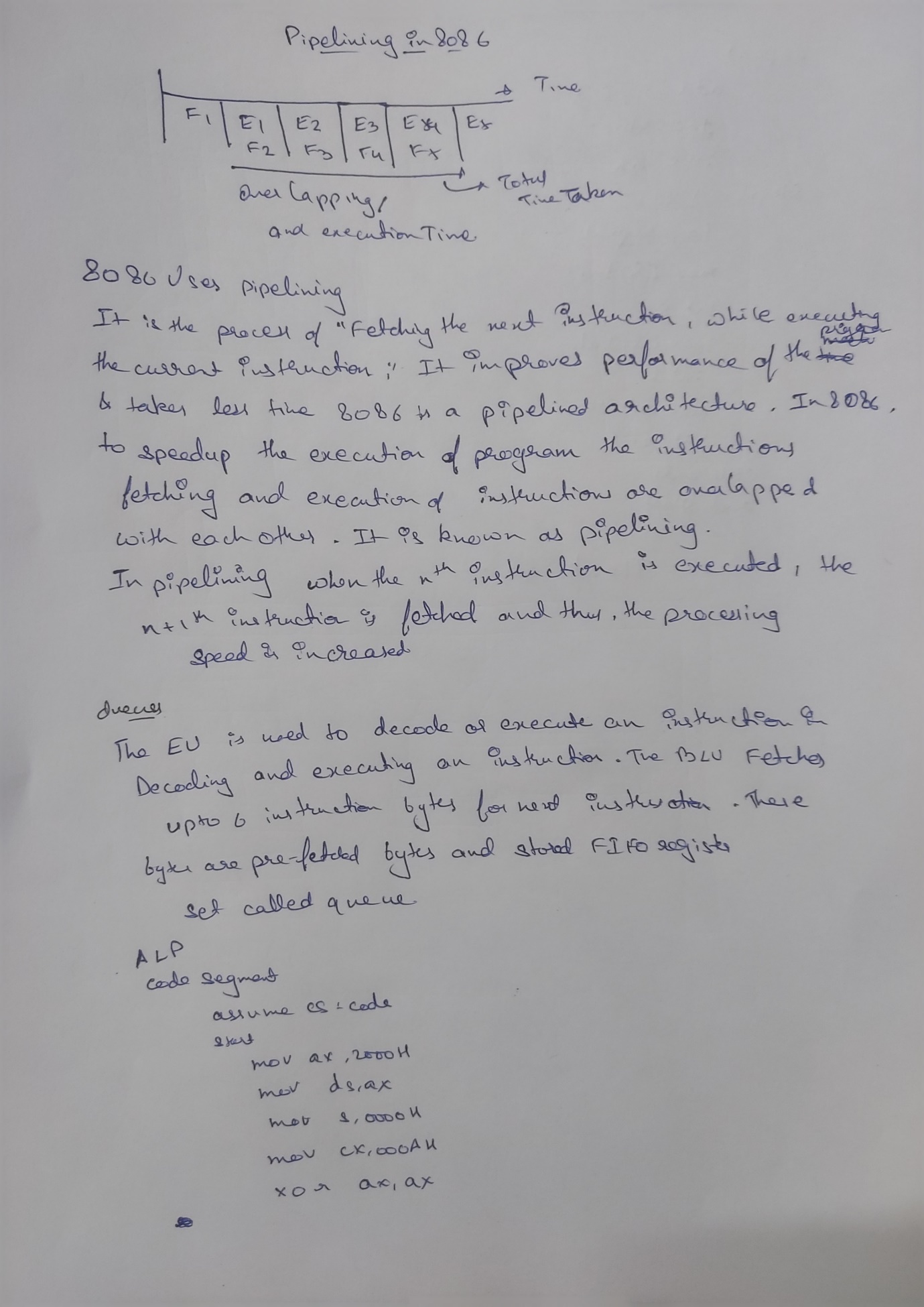
**to 20,009H. Store the result immediately after the series.**

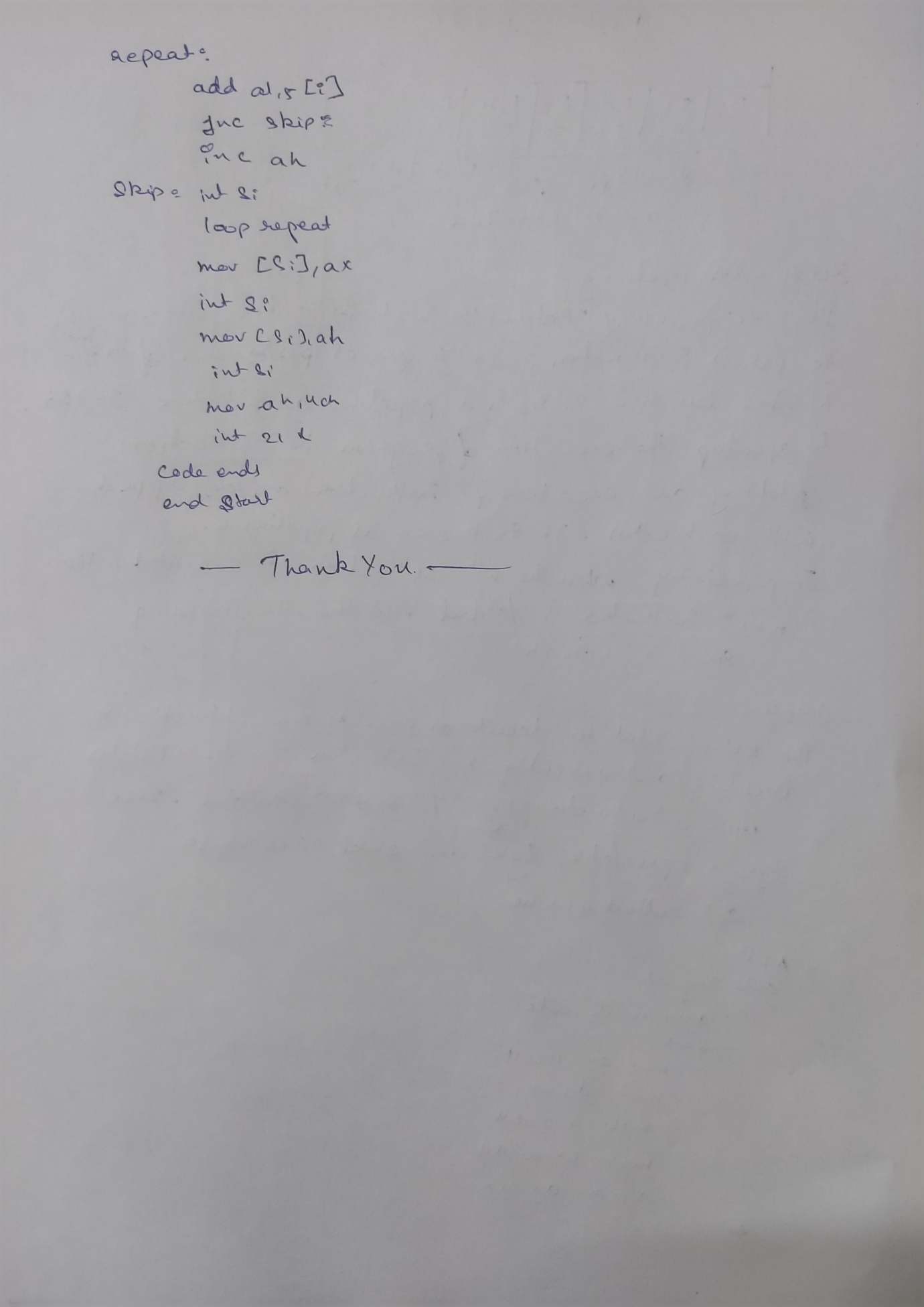
**Solution :**











**Thank You**